## R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

## COMPLETENESS OF THE OFFICE ACTION

Aside from a Notice of Allowance, Applicants' representative respectfully requests any further action on the merits be presented as a ***non-final*** action. 37 CFR §1.104(b) states:

> (b) *Completeness of examiner's action.* The examiner's ***action will be complete as to all matters***, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters of form need not be raised by the examiner until a claim is found allowable. (Emphasis added)

MPEP §706.07 further states:

> In making the final rejection, all outstanding ground of rejection of record should be carefully reviewed, and any such grounds relied on in the final rejection should be reiterated. They ***must also be clearly developed to such an extent that applicant may readily judge the advisability of an appeal*** unless a single previous Office action contains a complete statement supporting the rejection. (Emphasis added)

No arguments are presented in the current Office Action, or in any previous Office Action, why claim 7 is allegedly anticipated by Batchelor, U.S. Publication 2005/0025129. Applicants have never been provided with an opportunity to respond to the merits for the rejection of claim 7 since no Office Action has ever established a *prima facie* case to argue against. As such, the finality of the current Office Action is premature and should be withdrawn. If

neither a Notice of Allowance or a new non-final Office Action are issued, Applicants' representative respectfully requests the Examiner cite the authority for his actions and provide an explanation why 37 CFR §1.104(b) and MPEP §706.07 are not applicable.

**ANSWER ALL MATERIAL TRAVERSED**

Applicants' representative respectfully request that either a Notice of Allowance or a new Office Action on the merits be issued due to a lack of proper development for the rejection explanations. MPEP §707.07(f) states:

> In order to provide a complete application file history and to enhance the clarity of the prosecution history record, an examiner ***must provide clear explanations*** of all actions taken by the examiner during prosecution of an application.
> ...
> Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and ***answer the substance*** of it. (Emphasis added)

The current Office Action repeats the rejections for the following claims/steps, which were traversed by Applicants' representative. However, no answers to the substance of the traverses are provided in the current Office Action for the following:

1) Claims 1 and 14, step (A)

2) Claim 1, step (C)

3) Claim 14, step (B)

4) Claim 14, step (C)

5) Claim 2

6) Claim 3

7) Claim 4

8) Claim 6

9) Claim 7

10) Claim 8

11) Claim 9

12) Claim 10

13) Claim 11

14) Claim 12

15) Claim 13

16) Claim 16

17) Claim 17

As such, the current Office Action is incomplete and either a Notice of Allowance or a new Office Action should be issued. If neither a Notice of Allowance or a new Office Action are issued, Applicants' representative respectfully requests that the Examiner clearly cite the authority for his actions and provide an explanation why MPEP §707.07(f) is not applicable.

**CLAIM REJECTIONS UNDER 35 U.S.C. §102**

The rejection of claims 1-20 under 35 U.S.C. §102(e) as being anticipated by Batchelor, U.S. Patent Publication No. 2004/0025129A1 is respectfully traversed and should be withdrawn.

Batchelor concerns a system and methods for pre-artwork signal-timing verification of an integrated circuit design (Title).

The Federal Circuit has stated that "[t]o anticipate, ***every element and limitation*** of the claimed invention must be found

in a single prior art reference, ***arranged as in the claim.***"[1] (Emphasis added). The Federal circuit has added that the anticipation determination is viewed from one of ordinary skill in the art: "There must be ***no difference*** between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention."[2] (Emphasis added) Furthermore, "A claim is anticipated only if each and every element as set forth in the claim is found, either ***expressly or inherently described***, in a single prior art reference."[3] (Emphasis added) Furthermore, 37 C.F.R. §1.104(c)(2) states, "In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied upon must be designated as nearly as practicable. ***The pertinence of each reference, if not apparent, must be clearly explained*** and each rejected claim specified." (Emphasis added) The Federal Circuit also stated, "[I]n deciding the issue of anticipation, ***the trier of fact must*** identify the elements of the claims, determine their meaning in

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[1] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991) (Emphasis added by Appellant).

[2] *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

[3] *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, USPQ2d 1051, 1053 (Fed Circ. 1987).

light of the specification and prosecution history, and ***identify corresponding elements disclosed in the allegedly anticipating reference***."[4] (Emphasis added)

Claim 1 provides a step for (A) identifying a plurality of clock signals by analyzing a circuit design. Despite the assertion in the Office Action, element 475 in FIGS. 4 and 6 and the text in paragraph 0061 of Batchelor appear to be silent regarding a step for identifying clock signals by analyzing a circuit design. In particular, the clock buffer placements information 475 in FIGS. 4 and 6 of Batchelor do not appear to expressly or inherently describe (i) a plurality of clock signals, (ii) a circuit design and (iii) analyzing the circuit design to identify the plurality of clock signals. Paragraph 0061 of Batchelor reads:

> [0061] In addition, the timing constraints may be forwarded for application in a rules checker 470. The rules checker 470 may include logic configured to prevent a circuit designer and/or a circuit design team from storing a proposed circuit design that fails to meet one or more design criteria. Note that the design criteria applied by the rules checker 470 may include information regarding actual clock buffer placement 475 throughout the contemplated circuit (in lieu of designing the circuit under the assumption that **the clock signal** reaches each functional block across **the circuit** at the same time). The rules checker 470 may also include a time budget generator 620 and a constraint checker 625. (Emphasis added)

The above text mentions a circuit and **a single** clock signal. However, the above text does not appear to expressly or inherently describe (i) a plurality of clock signals, (ii) the circuit design

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[4] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481 at 485 (Fed. Cir. 1984).

being analyzed and (iii) a method step for identifying the plurality of clock signals. Therefore, Batchelor does not appear to disclose or suggest a step for (A) identifying a plurality of clock signals by analyzing a circuit design as presently claimed. As such, the Examiner is again respectfully requested to either (i) clearly and concisely explain how Batchelor allegedly describes a step for identifying a plurality of clock signals by analyzing a circuit design or (ii) withdraw the rejection.

Claim 1 further provides a step for (B) determining a plurality of relationships among the clock signals. Despite the assertion in the Office Action, FIGS. 1-4 and 6 and the text in paragraphs 0059 and 0061 of Batchelor appear to be silent regarding a step for determining a plurality of relationships among clock signals. In particular, FIGS. 1-4 and 6 of Batchelor do not appear to expressly or inherently describe any relationships among clock signals. FIG. 2 of Batchelor only shows a single clock signal. Paragraph 0061 of Batchelor, reproduced above, only mentions a single clock signal, but no (i) plurality of clock signals or (ii) a plurality of relationships among the plurality of clock signals. Paragraphs 0026-0029 and 0059 of Batchelor, read:

> [0026] The block diagrams and schematic presented in FIGS. 1-3 are provided to illustrate and describe aspects of computer-aided circuit design pertinent to the present invention. In this regard, FIG. 1 shows that an integrated circuit may be arranged and modeled with a plurality of separately defined functional blocks arranged and coupled in a hierarchical fashion across the integrated circuit. FIG. 2 illustrates the importance of tightly coordinating the relative timing between **clock** and data signals across an integrated circuit. Lastly, FIG. 3 presents a mechanism for

determining signal propagation time intervals for signals that traverse functional blocks within an integrated circuit.

[0027] FIG. 1 is a block diagram illustrating an integrated circuit representation 100 that may be generated in a computer-aided design tool. The integrated circuit representation 100 illustrated in FIG. 1 is grossly oversimplified for ease of illustration and discussion of aspects pertinent to the scope of the invention. It should be understood that VLSI circuits may contain tens to hundreds of millions of transistors and other various functional components. It should be further understood that an integrated circuit at that level of integration may be designed by individual circuit designers and/or by teams of circuit designers tasked with developing component arrangements to meet various functional and timing specifications. Thus, functional divisions or blocks may be assigned to various circuit designers or teams to design separate portions of the integrated circuit.

[0028] In this regard, the integrated circuit representation 100 includes circuit blocks labeled, A, B, and C. Circuit blocks A, B, and C may each contain circuitry configured to perform one or more designated functions for one or more time varying input signals. The circuit blocks A, B, and C may also be configured with appropriate conductors to forward output signals to each other and in some cases to destinations other than those on the integrated circuit 100. Circuit blocks A, B, and C are representative of a first level of the overall integrated circuit representation 100.

[0029] As shown in FIG. 1, circuit blocks B and C contain other circuit blocks. For example, circuit block B contains circuit blocks BA and BB. Circuit blocks BA and BB may be alternatively described as child blocks (of the parent-level block B) or second-level blocks. In this regard, the child or second-level blocks BA and BB are hierarchically arranged above the first level of the integrated circuit 100. Circuit block C contains child or second-level blocks CA, CB, and CC. In addition, block CA further includes child or third-level blocks CAA and CAB.

[0059] Reference is now directed to the functional block diagram of FIG. 6, which illustrates a representative design process 600 that can be implemented by the general-purpose computer 400 of FIG. 4. As illustrated in the design process 600, the timing analyzer 465 operative within the general-purpose computer 400 may be programmed to receive information from configuration file 452 and one or more netlist files 458 describing a present model of the contemplated VLSI circuit. The timing analyzer 465 may be

> programmed with a constraint generator 610. The constraint generator 610 receives relative timing information for signal interfaces as described above with regard to the representative circuit 300 illustrated and described FIG. 3. The constraint generator 610 applies the relative timing information to the identified interfaces conveyed in the configuration file 452 and the one or more netlists 458 to generate timing constraints that may be associated with each functional block of the contemplated circuit design. It should be understood that timing constraints may be generated and associated with each input signal that enters a functional block, as well as with each output signal that exits a functional block of interest. The timing constraints which may be defined as a relative portion of **a clock signal cycle** may be stored in memory 450 (FIG. 4) and/or communicated to each of the identified functional block designers. (Emphasis added)

The above text only appears to mention a single clock signal. Nothing in the above text appears to expressly or inherently describe (i) a plurality of clock signals or (ii) determining a plurality of relationships among the plurality of clock signals. Therefore, Batchelor does not appear to disclose or suggest a step for (B) determining a plurality of relationships among the clock signals as presently claimed. As such, the Examiner is again respectfully requested to either (i) clearly and concisely explain how Batchelor allegedly describes a step for determining a plurality of relationships among a plurality of clock signals or (ii) withdraw the rejection.

Claim 1 further provides a step for (C) generating a plurality of timing constraints for the circuit design in response to the clock signals and the relationships among the clock signals. Despite the assertion in the Office Action, elements 465 and 610 in FIG. 6 and the text in paragraphs 0059 and 0063 of Batchelor appear to be silent regarding a step for generating a plurality of timing

constraints for a circuit design in response to a plurality of clock signals and a plurality of relationships among the clock signals. In particular, the timing analyzer 465 and the constraint generator 610 in FIG. 6 of Batchelor do not appear to expressly or inherently describe generating a plurality of timing constraints in response to a plurality of clocks signals and a plurality of relationships among the clock signals. Paragraph 0059 of Batchelor, reproduced above, also does not appear to expressly or inherently describe (i) a plurality of clock signals and (ii) a plurality of relationships among the clock signals. Paragraph 0063 of Batchelor reads:

> [0063] The rules checker 470 may be programmed to highlight signal paths where potential timing flaws may occur in a runtime log file 454 and/or in an error/slack report 460. Furthermore, the rules checker 470 uses the schedule created by the time budget generator 620 to modify the circuit model. An updated circuit model may be partially reflected in binary file 462. As illustrated in FIG. 6, the binary file 462 may include a time budget 630 for each representation of the various functional blocks throughout the contemplated circuit.

Nowhere in the above text does Batchelor appear to expressly or inherently describe (i) a plurality of clock signals, (ii) a plurality of relationships among the clock signals or (iii) generating a plurality of timing constraints for a circuit design. Therefore, Batchelor does not appear to disclose or suggest a step for (C) generating a plurality of timing constraints for the circuit design in response to the clock signals and the relationships among the clock signals. Claim 20 provides language similar to claim 1. As such, the Examiner is again respectfully

requested to either (i) clearly and concisely explain how Batchelor allegedly describes a step for generating a plurality of timing constraints for a circuit design in response to a plurality of clock signals and a plurality of relationships among the clock signals or (ii) withdraw the rejection to claims 1 and 20.

Claim 20 further provides a structure comprising a medium and a computer program recorded in the medium. In contrast, the Office Action makes no arguments and provides no evidence that Batchelor describes elements similar to the claimed medium and the claimed computer program. Therefore, *prima facie* anticipation has not been established. As such, the Examiner is respectfully requested to either (i) clearly identify elements of Batchelor allegedly similar to the claimed medium and the claimed computer program or (ii) withdraw the rejection.

Claim 14 provides a step for (A) identifying a plurality of clock signals by analyzing a circuit design. Despite the assertion in the Office Action, the element 475 in FIGS. 4 and 6 and the text in paragraph 0061 of Batchelor appear to be silent regarding a plurality of clock signals. As argued above for claim 1, FIGS. 4 and 6 and paragraph 0061 of Batchelor do not appear to expressly or inherently describe (i) a plurality of clock signals, (ii) identifying a plurality of clock signals and (iii) analyzing a circuit design. Therefore, Batchelor does not appear to disclose or suggest a step for (A) identifying a plurality of clock signals by analyzing a circuit design as presently claimed. As such, the Examiner is again respectfully requested to either (i) clearly and

concisely explain how Batchelor allegedly describes a step for identifying a plurality of clock signals by analyzing a circuit design or (ii) withdraw the rejection.

Claim 14 further provides a step for (B) querying a user for a plurality of parameters for the clock signals. Despite the assertion in the Office Action, FIGS. 1-4 and 6 and paragraphs 0026-0029, 0059 and 0061, all paragraphs reproduced above, appear to be silent regarding (i) a plurality of clock signals, (ii) querying a user and (iii) a plurality of parameters for the clock signals. Furthermore, no arguments are provided in the Office Action regarding the querying step of claim 14. Therefore, Batchelor does not appear to disclose or suggest a step for (B) querying a user for a plurality of parameters for the clock signals as presently claimed. As such, the Examiner is again respectfully requested to either (i) provide evidence and arguments how Batchelor allegedly anticipates the claimed step or (ii) withdraw the rejection.

Claim 14 further provides a step for (C) generating a plurality of timing constraints in response to a plurality of clock signals and a plurality of parameters. Despite the assertion in the Office Action, elements 465 and 610 in FIG. 6 of Batchelor and paragraphs 0059 and 0063 of Batchelor, all paragraphs reproduced above, appear to be silent regarding (i) a plurality of clock signals, (ii) a plurality of parameters queried from a user and (iii) generating timing constraints in response to the clocks and the parameters. Furthermore, the Office Action makes no arguments

that Batchelor allegedly mentions generating timing constraints in response to a plurality of parameters for a plurality of clock signals queried from a user. Therefore, Batchelor does not appear to disclose or suggest a step for (C) generating a plurality of timing constraints in response to a plurality of clock signals and a plurality of parameters as presently claimed. Claim 21 provides language similar to claim 14. As such, the Examiner is again respectfully requested to either (i) provide evidence and arguments how Batchelor allegedly anticipates the claimed step or (ii) withdraw the rejection to claims 14 and 21.

Claim 21 further provides a structure comprising a medium and a computer program recorded in the medium. In contrast, the Office Action makes no arguments and provides no evidence that Batchelor describes elements similar to the claimed medium and the claimed computer program. Therefore, *prima facie* anticipation has not been established. As such, the Examiner is respectfully requested to either (i) clearly identify elements of Batchelor allegedly similar to the claimed medium and the claimed computer program or (ii) withdraw the rejection.

Claim 2 provides that the plurality of clock signals comprise a test clock signal. Despite the assertion in the Office Action, FIGS. 4 and 6 of Batchelor and the text in paragraphs 0059 and 0061 of Batchelor, all paragraphs reproduced above, appear to be silent regarding a test clock signal. The Examiner mentioned, during a phone conversation on June 29, 2005, that paragraph 0062

of Batchelor discusses test clocks. Paragraph 0062 of Batchelor reads:

> [0062] The time budget generator 620 may be configured to convert available time constraints into a schedule that describes signal-timing relationships at the functional block borders. The constraint checker 625 may be configured to check the various signal paths to identify paths where a potential timing flaw or overlap may occur. Input signal overlaps may be identified where the sum of an expected boundary arrival time and an acceptable uncertainty factor does not leave the functional block enough time to generate and transmit the desired output signals at the output ports. Output signal overlaps may be identified where the sum of processing time for a particular functional block of interest and an acceptable transmit uncertainty factor (and in some cases a relatively late input signal arrival time) result in an output signal that does not reach the output port of the functional block within the allotted time slot.

Nowhere in the above text, or in any other section, does Batchelor appear to expressly mention test clock signals. Therefore, Batchelor does no appear to disclose or suggest that the plurality of clock signals comprise a test clock signal as presently claimed. As such, the Examiner is again respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly describes a test clock signal or (ii) withdraw the rejection.

Claim 3 provides a step of eliminating a respective timing constraint of a plurality of timing constraints for each signal connected to an internal pin for a circuit design that defines a non-clock signal. Despite the assertion in the Office Action, FIG. 6 and the text in paragraphs 0060 and 0061 of Batchelor appear to be silent regarding a step for eliminating from a plurality of timing constraints. In particular, paragraph 0061 of Batchelor, reproduced above, does not appear to expressly or

inherently describe eliminating timing constraints. Paragraph 0060 of Batchelor reads:

> [0060] In turn, each functional block circuit designer or circuit design team may from time to time during the design process adjust the constraints. For example, a particular functional block design may receive an input signal substantially sooner than was previously indicated. As a result, one or more output signals forwarded from the functional block may reach the output ports of the functional block at an earlier point in the clock cycle, thus permitting more time for designers of subsequent blocks to complete their respective signal processing. Alternatively, a particular functional block design may receive an input signal in accordance with previous timing constraints. However, for various reasons, the designer may be unable to complete the necessary logic processing within the allotted time. For situations where a designer or design team adjusts the timing constraints, it is desired that the timing analyzer 465 receive the latest timing constraints used by the various functional block designers to determine if possible signal timing flaws may be introduced if the final circuit design were to function in accordance with the present design of the functional blocks.

Nowhere in the above text, or in any other section, does Batchelor appear to expressly or inherently describe (i) signals connected to internal pins for a circuit design that defines non-clock signals or (ii) eliminating a respective timing constraint for such signals. Therefore, Batchelor does not appear to disclose or suggest a step of eliminating a respective timing constraint of a plurality of timing constraints for each signal connected to an internal pin for a circuit design that defines a non-clock signal as presently claimed. Claim 4 provides language similar to claim 3. As such, the Examiner is again respectfully requested to either (i) clearly and concisely explain how Batchelor allegedly describes a step for eliminating from a plurality of timing constraints or (ii) withdraw the rejections of claims 3 and 4.

Claim 5 provides that the step (C) for generating a plurality of timing constraints is in further response to a plurality of parameters associated with the plurality of clock signals. Despite the assertion in the Office Action, paragraphs 0061, reproduced above, and 0064 of Batchelor do not appear to expressly or inherently describe (i) a plurality of clock signals, (ii) a plurality of parameters for the plurality of clock signals and (iii) generating timing constraints in response to the parameters. Paragraph 0064 of Batchelor reads:

> [0064] FIG. 7 is a flow diagram illustrating a representative method 700 for time-budgeting an integrated circuit representation such as the integrated circuit representation 100 of FIG. 1. As illustrated in the flow diagram, a general-purpose computer 400 configured to implement the method 700 for time-budgeting may begin by initializing the system. Step 702 may include loading a plurality of model (i.e., data) files. These files may include the configuration file 452, previously generated timing models 455, netlist files 458, technology file 453, and the parasitics file 456 among others. As described above, the plurality of data files are used to formulate a hierarchically arranged model of the various signal paths that associate the various functional blocks of the modeled circuit. Ultimately, the model will describe signal timing (relative to **a clock signal**) for each signal that traverses each of the defined functional blocks of the modeled circuit. For a hierarchically arranged circuit, the timing analyzer 465 (FIG. 4) is applied over the various hierarchical levels to establish the timing constraints that the circuit designers of functional blocks should meet to ensure the intended operation of the circuit as a whole. The **clock signal** at each functional block may be modeled by information that includes the clock period and clock signal uncertainty. Additional information may include clock and data signal transition limits. Next, as shown in step 704, the general-purpose computer 400 may be programmed to prompt the user to set a hierarchy level of interest. (Emphasis added)

Nowhere in the above text, or in any other section, does Batchelor appear to expressly or inherently describe (i) a plurality of

parameters for a plurality of clock signals and (ii) generating timing constraints in response to the clock signals and parameters. Therefore, Batchelor does not appear to disclose or suggest that the step (C) for generating a plurality of timing constraints is in further response to a plurality of parameters associated with the plurality of clock signals as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly explain how Batchelor allegedly describes a plurality of parameters for a plurality of clocks being used to generate timing constraints or (ii) withdraw the rejection.

Claim 6 provides that at least one of a plurality of parameters relates to a test clock signal. Despite the assertion in the Office Action, the text in paragraphs 0016 and 0064 of Batchelor do not appear to expressly or inherently describe a test clock signal. Paragraph 0064 of Batchelor is reproduced above. Paragraph 0016 of Batchelor reads:

> [0016] Other systems, methods, and features of the present invention will be or become apparent to one skilled in the art upon examination of the following drawings and detailed description. It is intended that all such additional systems, methods, and features are included within this description, are within the scope of the present invention, and are protected by the accompanying claims.

Nowhere in the above paragraphs, or in any other section, does Batchelor appear to expressly or inherently mention a test clock signal. Therefore, Batchelor does not appear to disclose or suggest that at least one of a plurality of parameters relates to a test clock signal as presently claimed. As such, the Examiner is again respectfully requested to either (i) clearly and concisely

identify where Batchelor allegedly describes a test clock signal and a related parameter or (ii) withdraw the rejection.

Claim 7 provides a step for eliminating a respective timing constraint of a plurality of timing constraints for each signal of a circuit design that defines a static signal. In contrast, the Office Action provides no evidence or arguments that Batchelor anticipates the claimed step. In particular, the cites to "fig 1-5 col 2 lines 23-61 and col 3 lines 16 to col 4 lines 64" is a residue from the first Office Action citing figures and text of Ginetti et al. '658. Therefore, *prima facie* anticipation has not been established. As such, the Examiner is again respectfully requested to either (i) provide ***a new non-final Office Action*** with evidence and agreements how Batchelor allegedly anticipates the claimed step or (ii) withdraw the rejection.

Claim 8 provides that the step (B) for determining a plurality of relationships among a plurality of clock signals comprises a sub-step of generating an asynchronous relationship of the relationships between at least two of the clock signals operating asynchronously to each other. Despite the assertion in the Office Action, the FIGS. 4 and 6 and the text in paragraphs 0059 and 0061 of Batchelor, all paragraphs reproduced above, do not appear to expressly or inherently describe (i) at least two clock signals operating asynchronously to each other or (ii) generating an asynchronous relationship between the at least two clock signals. Therefore, Batchelor does not appear to disclose or suggest that the step (B) for determining a plurality of

relationships among a plurality of clock signals comprises a sub-step of generating an asynchronous relationship of the relationships between at least two of the clock signals operating asynchronously to each other as presently claimed. As such, the Examiner is again respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly describes at least two clock signals operating asynchronously to each other or (ii) withdraw the rejection.

Claim 9 provides that the step (B) further comprises a sub-step of generating a fastest clock relationship of the relationships between at least two of the clock signals operating at different speeds between two clock boundaries of the circuit design. Despite the assertion in the Office Action, FIGS. 4 and 6 and the text in paragraphs 0059 and 0061 of Batchelor, all paragraphs reproduced above, do not appear to expressly or inherently describe at least two clock signals operating at different speeds between two clock boundaries. Therefore, Batchelor does not appear to disclose or suggest that the step (B) further comprises a sub-step of generating a fastest clock relationship of the relationships between at least two of the clock signals operating at different speeds between two clock boundaries of the circuit design as presently claimed. As such, the Examiner is again respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly describes at least two clock signals operating at different speeds between two clock boundaries or (ii) withdraw the rejection.

Claim 10 provides that the step (B) further comprises a sub-step of generating a multiplexed clock relationship of the relationships between at least two of the clock signals routable through a multiplexer in the circuit design. Despite the assertion in the Office Action, FIGS. 4 and 6 and the text in paragraphs 0059 and 0061 of Batchelor, all paragraphs reproduced above, do not appear to expressly or inherently describe at least two of the clock signals routable through a multiplexer. Therefore, Batchelor does not appear to disclose or suggest that the step (B) further comprises a sub-step of generating a multiplexed clock relationship of the relationships between at least two of the clock signals routable through a multiplexer in the circuit design as presently claimed. As such, the Examiner is again respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly describes (a) a multiplexer and (b) two clock signals routed through the multiplexer or (ii) withdraw the rejection.

Claim 11 provides that the step (B) further comprises a sub-step of generating a derivative clock relationship of the relationships between a first of the clock signals that is derived from a second of the clock signals. Despite the assertion in the Office Action, the text in paragraphs 0059 and 0061 of Batchelor, reproduced above, do not appear to expressly or inherently describe a first clock signal derived from a second clock signal. Therefore, Batchelor does not appear to disclose or suggest that the step (B) further comprises a sub-step of generating a derivative clock relationship of the relationships between a first

of the clock signals that is derived from a second of the clock signals as presently claimed. As such, the Examiner is again respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly describes a first clock signal derived from a second clock signal and generates a derivative clock relationship or (ii) withdraw the rejection.

Claim 12 provides that the step (B) further comprises a sub-step of generating a shared structure relationship of the relationships between a test clock signal of the clock signals and a normal clock signal of the clock signals, each driving a particular structure of the circuit design in different modes for the circuit design. Despite the assertion in the Office Action, FIGS. 4 and 6 and the text in paragraphs 0059 and 0061 of Batchelor, all paragraphs reproduced above, do not appear to expressly or inherently describe (a) a shared structure relationship, (b) a test clock signal, (c) a particular structure of a circuit design and (d) different modes. Therefore, Batchelor does not appear to disclose or suggest that the step (B) further comprises a sub-step of generating a shared structure relationship of the relationships between a test clock signal of the clock signals and a normal clock signal of the clock signals, each driving a particular structure of the circuit design in different modes for the circuit design as presently claimed. As such, the Examiner is again respectfully requested to either (i) clearly and concisely explain how Batchelor allegedly describes (a) a shared structure relationship, (b) a test clock signal, (c) a particular

structure of a circuit design and (d) different modes or (ii) withdraw the rejection.

Claim 13 provides a step for writing a plurality of timing constraints among a plurality of files. Despite the assertion in the Office Action, the text in paragraphs 0016 and 0064 of Batchelor, reproduced above, do not appear to expressly or inherently describe writing timing constraints among a plurality of files. Therefore, Batchelor does not appear to disclose or suggest a step for writing a plurality of timing constraints among a plurality of files as presently claimed. As such, the Examiner is again respectfully requested to either (i) clearly and concisely explain how Batchelor allegedly describes (a) a plurality of files and (b) a step for writing timing constraints among the files or (ii) withdraw the rejection.

Claim 16 provides a step for querying a user for a frequency parameter for each of the clock signals. Despite the assertion in the Office Action, the text in paragraphs 0016 and 0064 of Batchelor, reproduced above, do not appear to expressly or inherently describe querying a user for parameters. Therefore, Batchelor does not appear to disclose or suggest a step for querying a user for a frequency parameter for each of the clock signals. Claim 17 provides language similar to claim 16. As such, the Examiner is again respectfully requested to either (i) clearly and concisely identify where Batchelor allegedly describes a step for querying a user or (ii) withdraw the rejections for claims 16 and 17.

Claims 18 and 19 depend from claim 14, which is now believed to be allowable. Since the dependent claims contain all of the limitations of the independent claim, claims 18 and 19 are fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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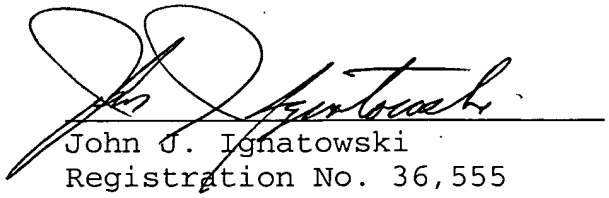

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